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# Netlist Powered Emulation Paradigm: Pioneering Breakthroughs in Gate Level Verification


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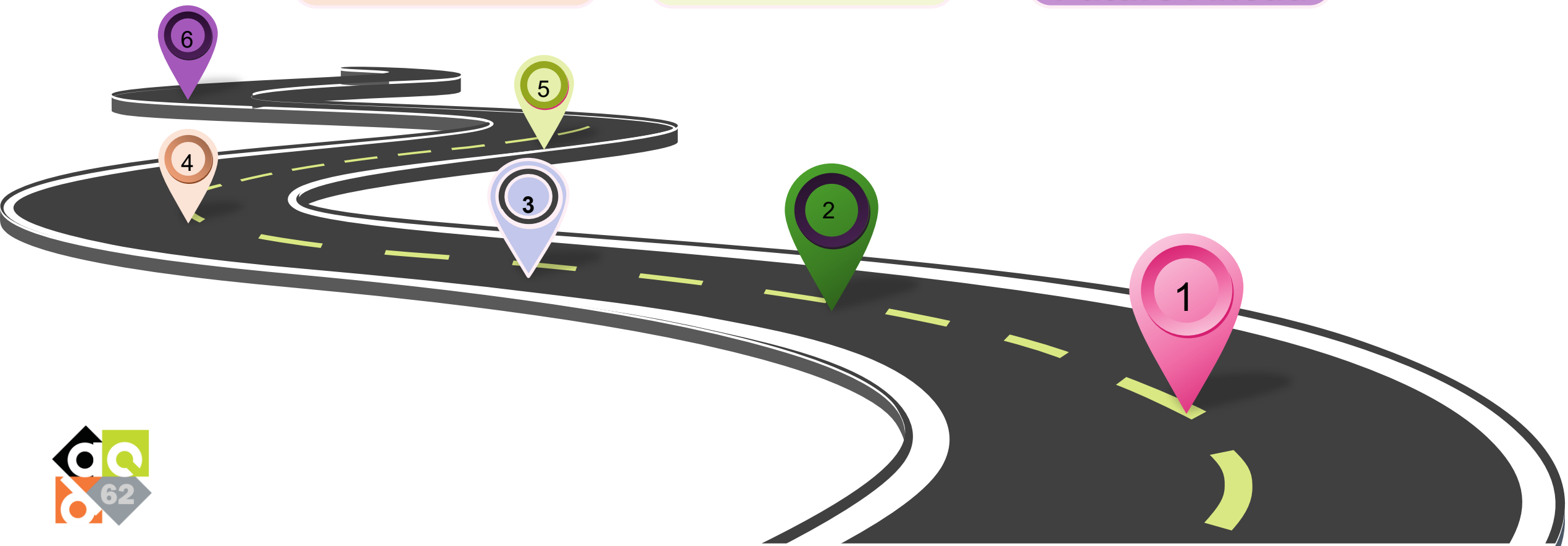


# Motivation

- Growth in Semiconductor Industry
- Rapidly increasing complexity in modern SoC designs
- Ensuring maximum verification coverage with No bug escape
- Challenge to Validate chip on time

**Gate Level Simulation:**

❑Conventional gate level simulation is widely employed.
❑High run time
❑Challenge to run Full SoC GLS Simulation

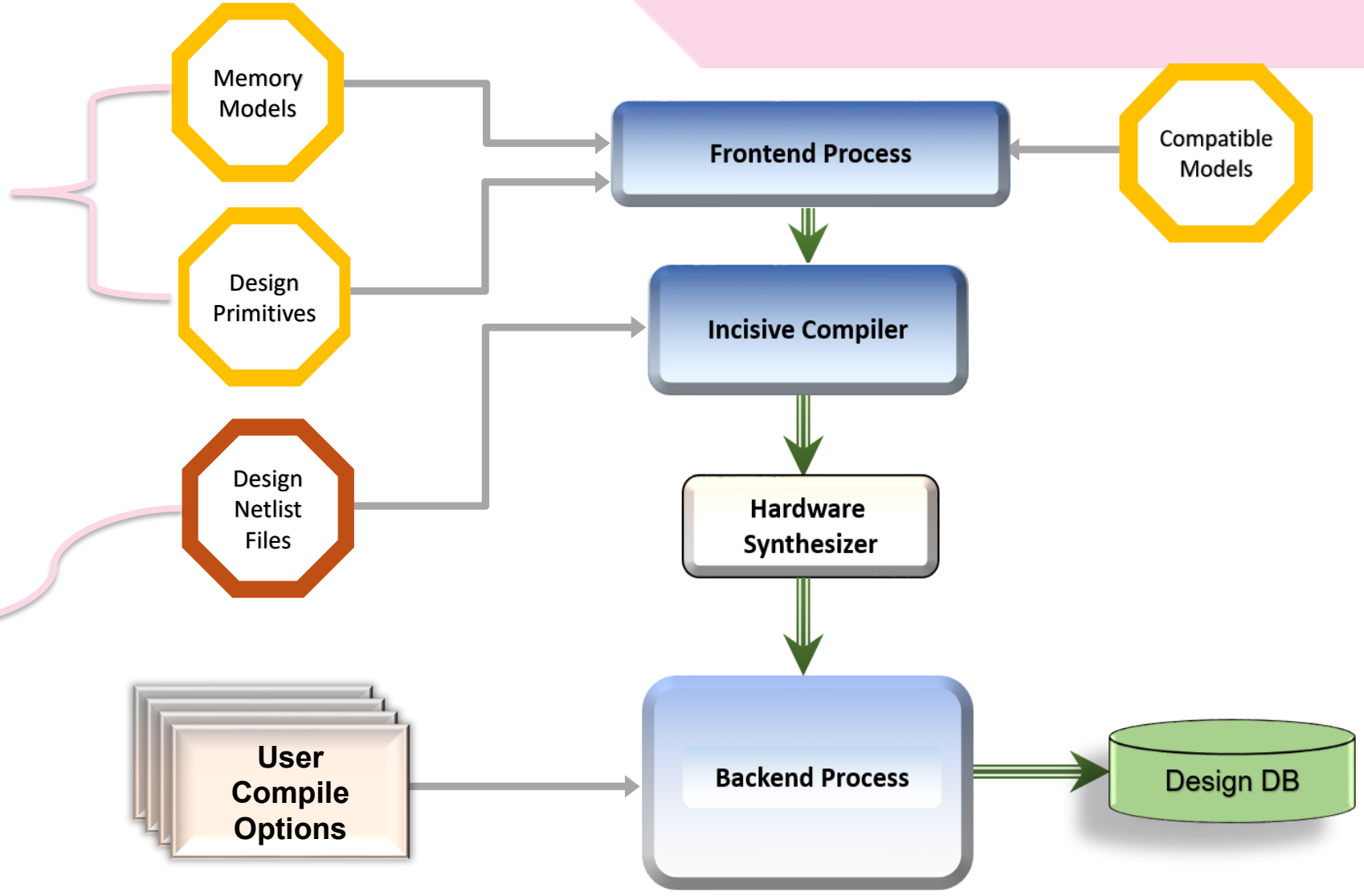
**Netlist Powered Emulation:**

❑Adopting to Zero delay netlist powered emulation
❑Shorter run time
❑ Full SoC GLE is faster
❑Execution of system level scenarios

# Netlist Powered Emulation Paradigm- Methodology

All the required directive files are to be passed in the Frontend process stage for Analysis, Elaboration, Optimization

Inclusion of Netlist files at the Incisive Compiler stage by-passing the Front end process



# Netlist Powered Emulation Paradigm- Enhancement Techniques

- Several Optimization strategies are proposed and devised to enhance our platform.

1) **<u>Compile Time Enhancement Techniques</u>:**

   **Explicit Netlist Flow**

2) **<u>Performance Enhancement Techniques</u>:**

   **Oversampling Technology**
   **Handling and Breaking Long Signal Paths**

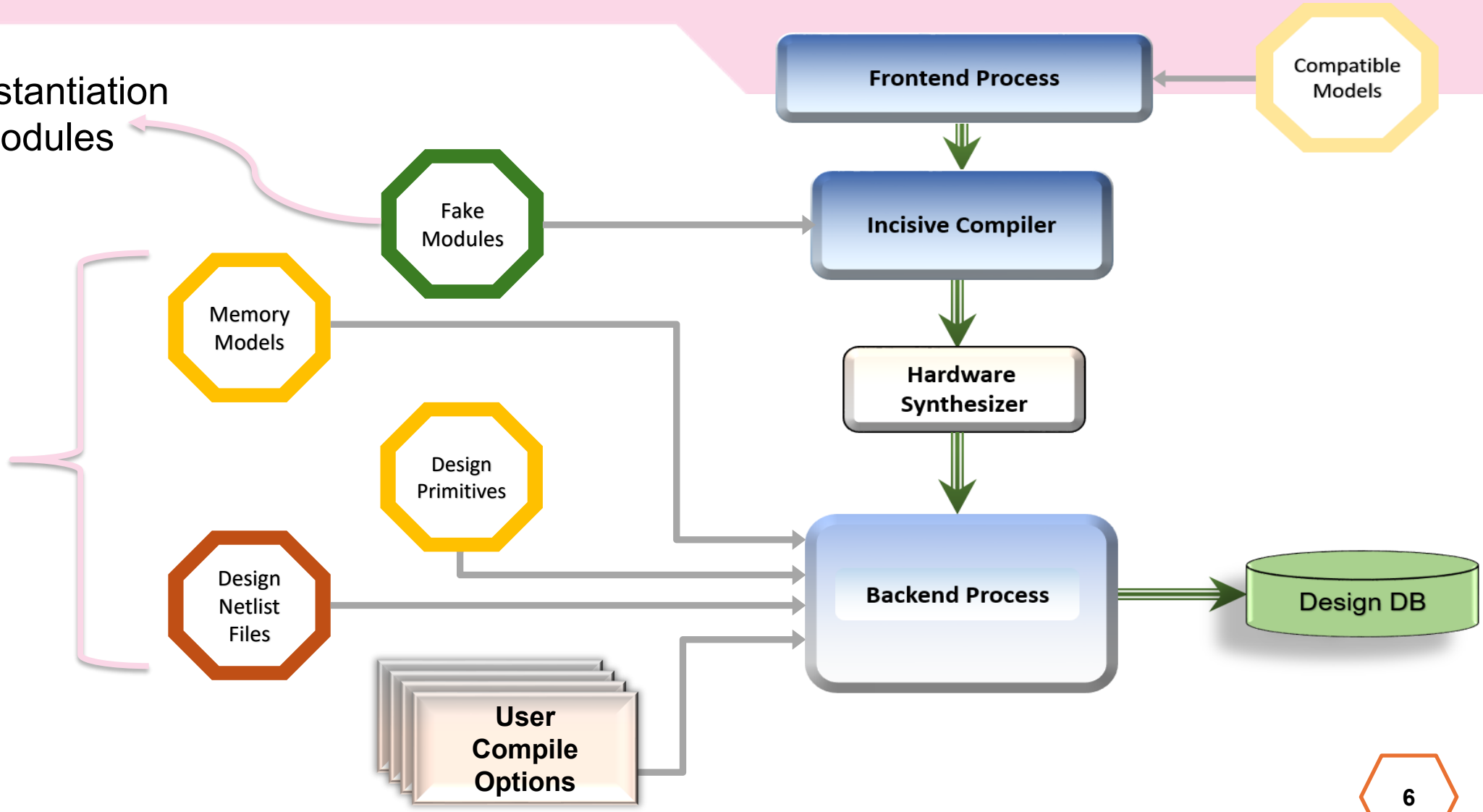
3) **<u>Smarter Enhancement Techniques</u>:**

   **Hybrid and Stub Approach**

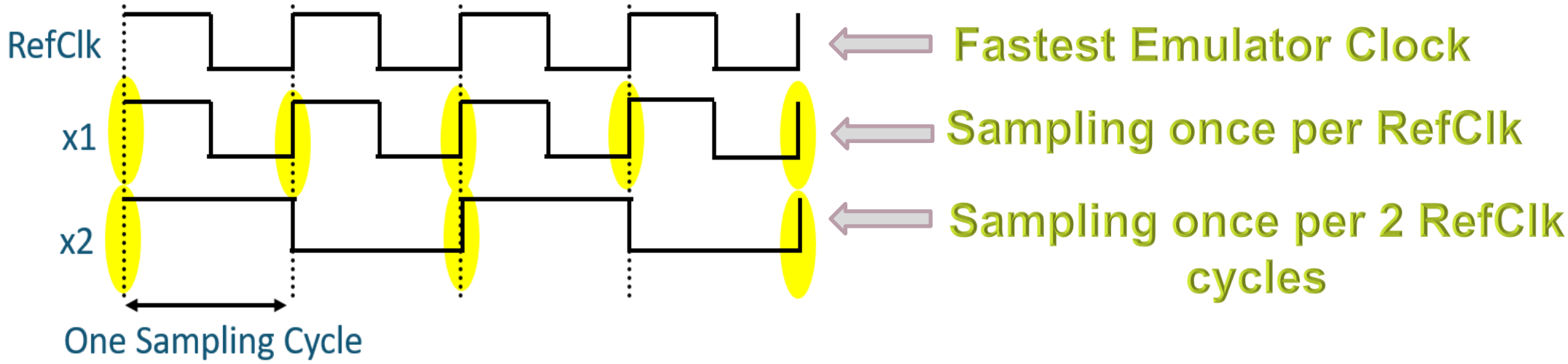
# Compile Time Enhancement – Explicit Flow

Stubbed Instantiation of the modules

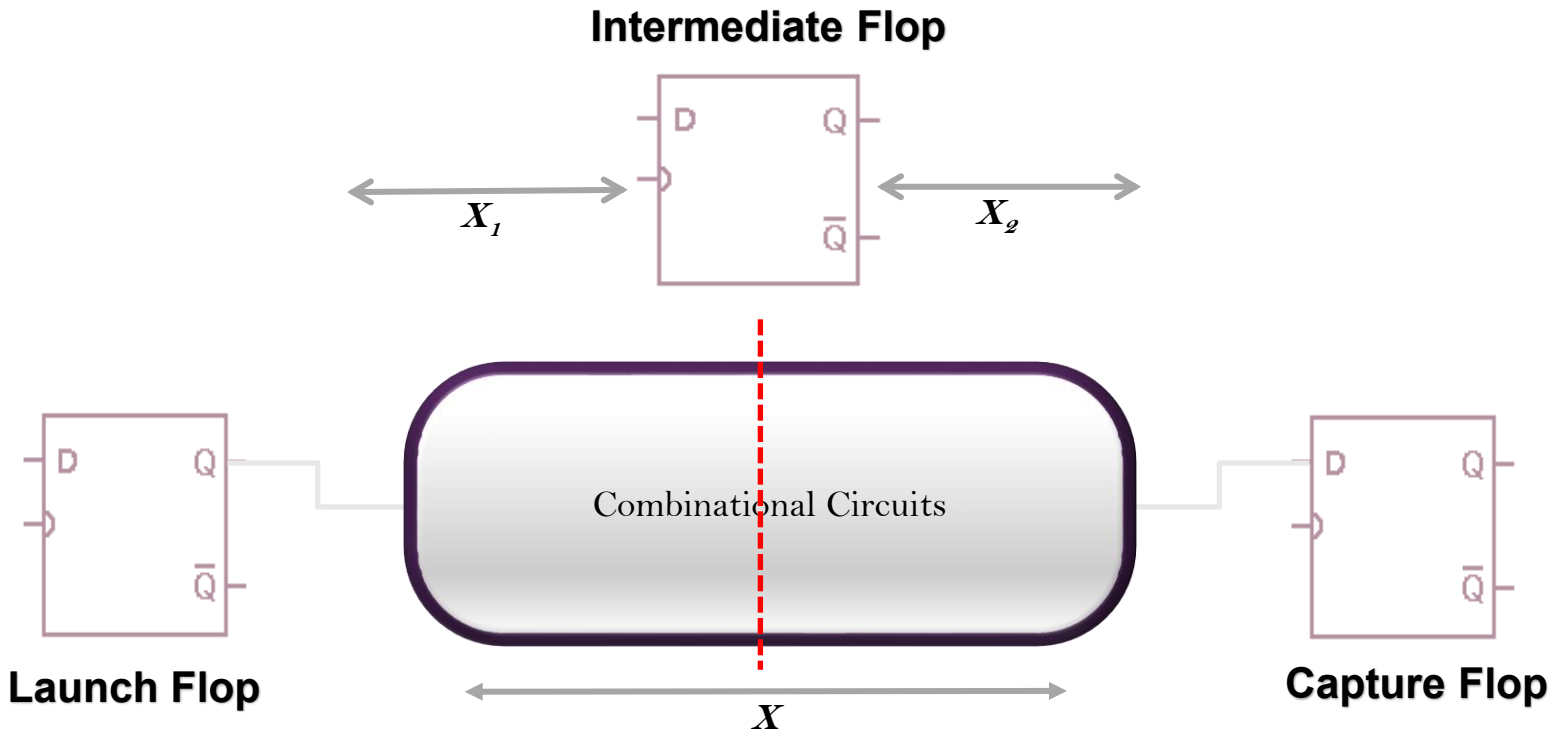
Importing directly at the backend process bypassing all the front-end stages.



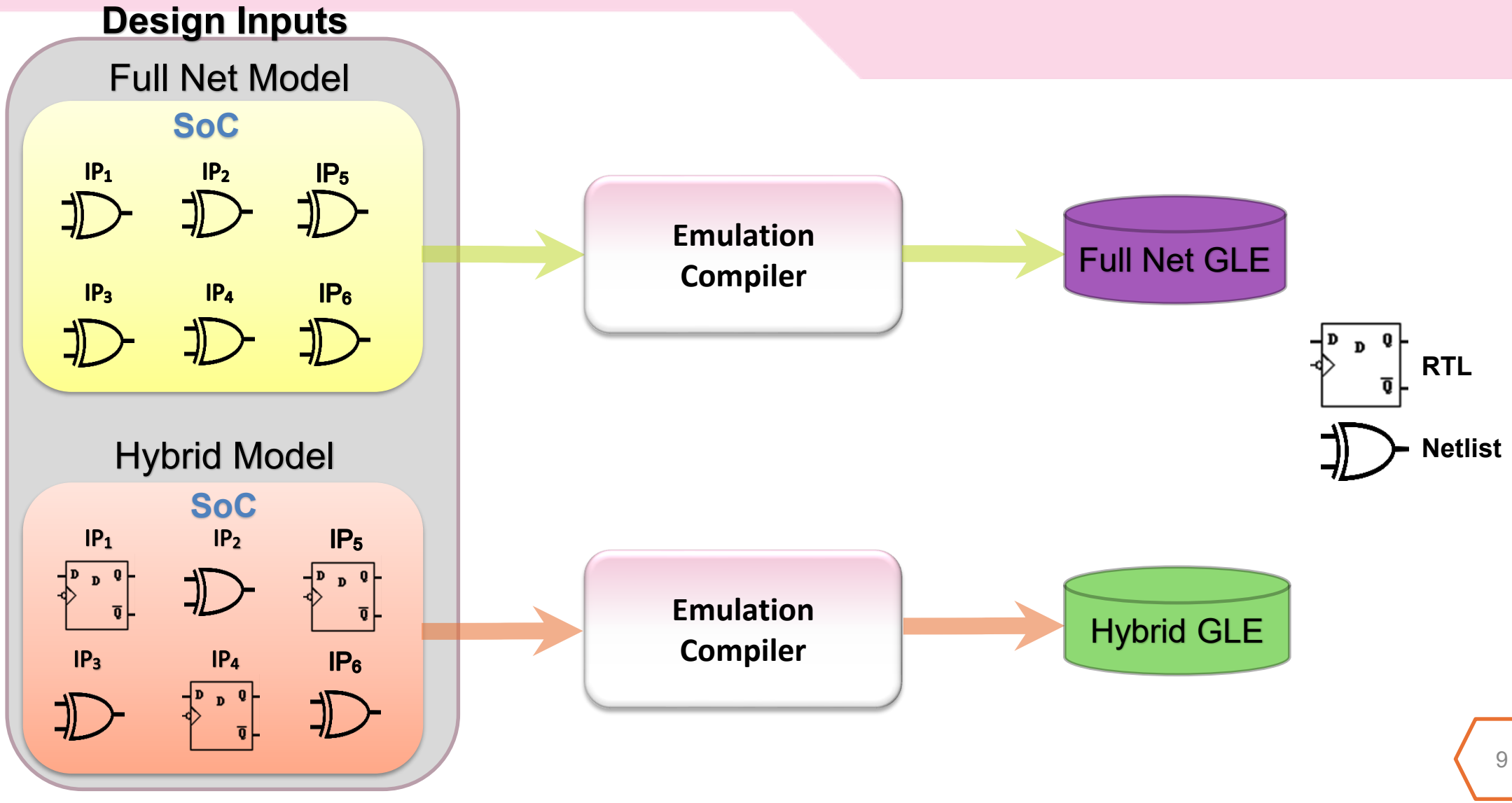
# Performance Enhancement - Oversampling



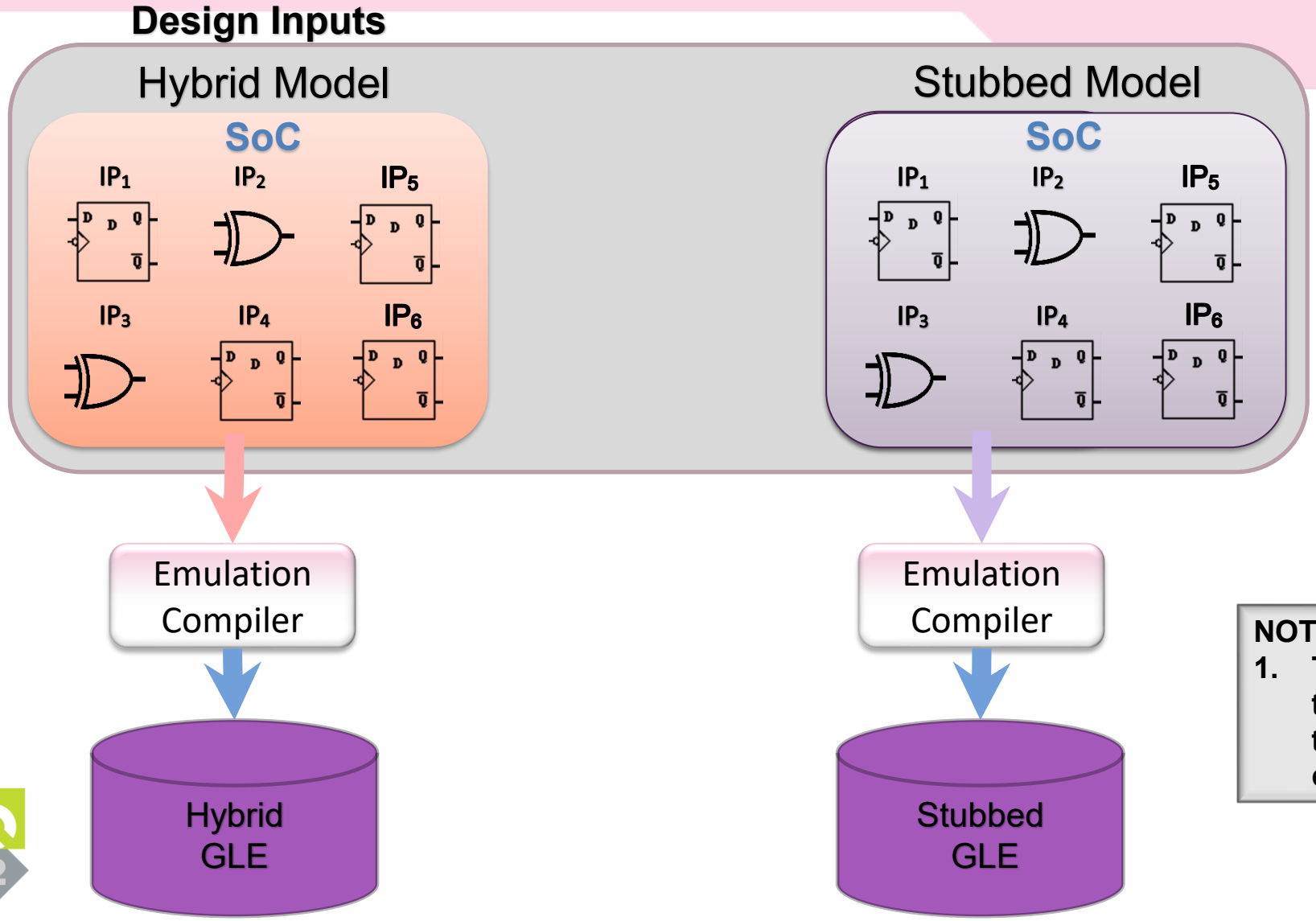
# Performance Enhancement – Handling Long Paths

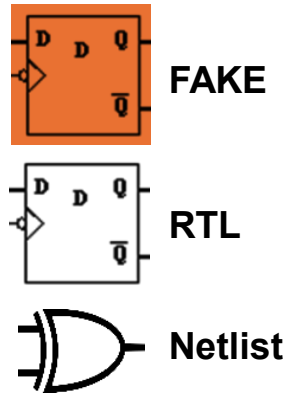


# Smarter Solutions – Hybrid GLE



# Smarter Solutions – Stubbed GLE



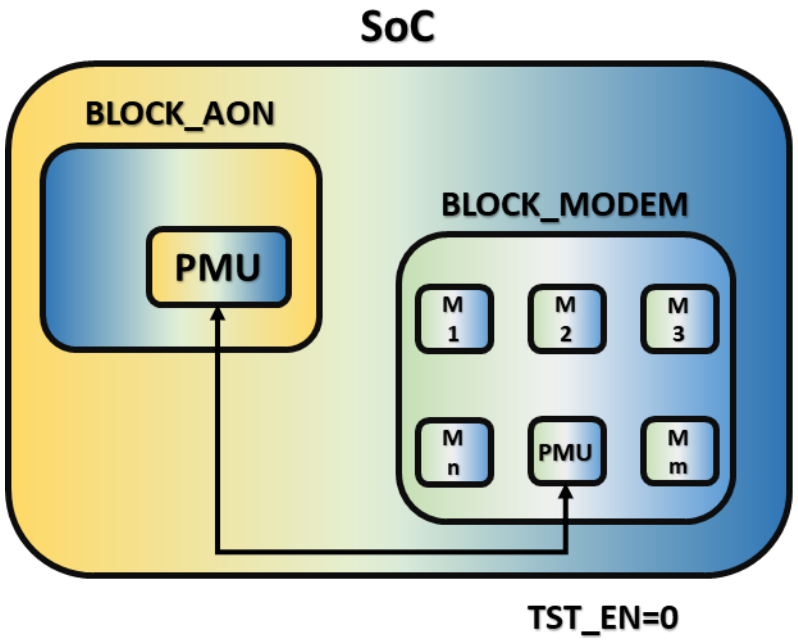




**NOTE:**

1. **Third party blocks are handled after thorough hardening and making them compatible to the design compiler.**

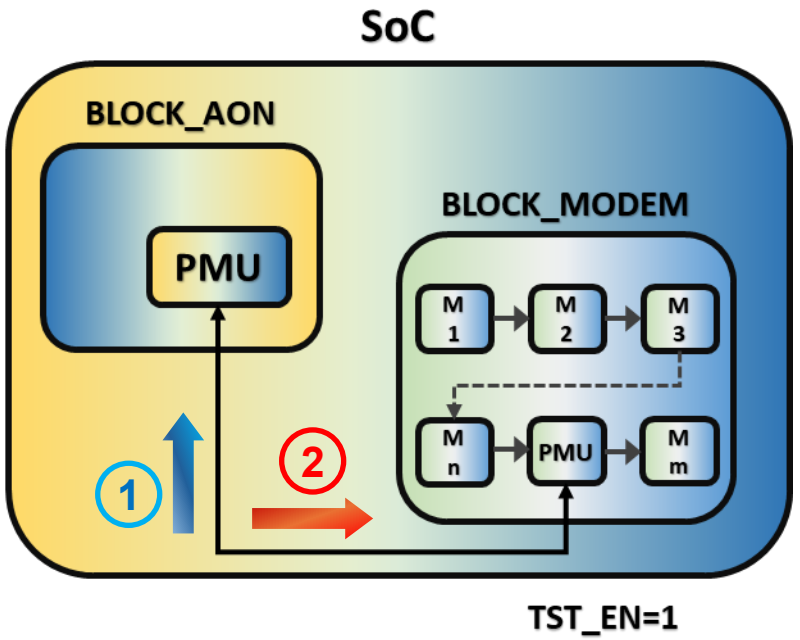
# Evidence/ Potential Bugs Caught

## Functional Mode




Handshake between SoC PMU and BLK_MODEM PMU to ensure the modem is powered up and operates correctly

## Test Mode




All IPs within the BLK_MODEM are interconnected to form a scan chain

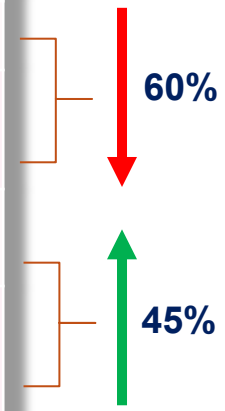
1) During Scanning, unexpected interaction inadvertently triggers a transaction to the SoC PMU

2) SoC PMU processes transaction. Resulting in the blk_modem power down unexpectedly, disrupting its functionality

# Results Summary-Compile and Run

Table I. Anticipated outcomes of verification stages on different design types and across various range of emulators

| Verification Stage | Design Type | SoC (2Billion Gates) | | |
|---|---|---|---|---|
| | | GLS | FPGA | ASIC |
| Compile Duration (Hrs) | FULL NET | 18 hrs | 25 hrs | 15 hrs |
| | Adopting Techniques | 15 hrs | 20 hrs | 9 hrs |
| Operating Speed (KHz) | FULL NET | - | 1400 khz | 300 khz |
| | Adopting Techniques | - | 1900 khz | 700 khz |




NOTE: Based on the application requirements, the design can be tweaked further with the smarter solutions to improve the performance and reduce the compile time

# Results Summary-Run Examples

Table II. Proposed Execution Time Comparison on Gate Level Simulation vs Netlist Powered Emulation

| Applications | Gate Level Simulation (Hrs) | Netlist Powered Emulation (Hrs) |
|---|---|---|
| SoC Boot | 14 | 0.1 |
| Dynamic Power Analysis | 50 | 1.5 |
| Scan Validation | Unrealistic | 2 |
| LBIST | Unrealistic | 4 |

# Limitations & Future Ahead …

## Limitations

- Only Zero delay/ Unit delay as timing simulation is not supported.
- When test modes are enabled, emulator driver clock drops significantly.
- Netlists have to undergo front-end process in a FPGA based compiler.

## Future Ahead

- Power Aware GLE (2 State, 4 State)
- DFT scenarios Validation

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